

**REMARKS/ARGUMENTS**

Claims 17 - 33 are pending.

The specification has been amended to indicate that priority is being claimed from Japanese Application No. 2000-371486, filed December 1, 2000 and Japanese Application No. 2000-381652, filed December 11, 2000.

Drawings objections were raised. Drawing corrections have been made. As for Figs. 1 and 3, mention of reference numeral 310 is made in the specification as amended. As for Figs. 10A through 10D, these figures do not constitute prior art, but rather are illustrations of the effect of the present invention. Figs. 10A and 10C represent burst error patterns to which the present invention is applied. Figs. 10B and 10D illustrate the result of applying the invention respectively to Fig. 10A and 10C. Kindly refer to the specification as originally filed on page 11, line 25 to page 12, line 4 and lines 12 - 19.

The specification was objected to for grammatical and idiomatic errors. The specification has been reviewed and amended to correct for grammatical and idiomatic errors. A mark-up copy of the specification showing the amendments and a clean-copy substitute specification are submitted herewith. No new matter has been added.

The original claims 1 - 6 were objected to and rejected under 35 U.S.C. Sections 112 and 103. The claims 1 - 16 have been cancelled without prejudice or disclaimer. Claims 17 - 33 have been appended.

The present invention is directed to data recording and reproduction on a recording medium. Aspects of the invention as recited in independent claim 17 include "forming a data block organized as a plurality of first data columns arranged in a plurality of rows." For each row, "a plurality of second columns [is added] to include an error correcting code parity." Further for each row "rearranging an order of bytes of said first data columns according to two or more rearranging rules." See also independent claim 29.

Dependent claims 25 - 27 recite aspects related to a specific format of recording medium, namely, digital versatile disc (DVD).

Independent claims 28 and 33 recite data reproduction aspects of the present invention. A data block is formed “including a plurality of first data columns stacked in a plurality of rows, each first data column including a plurality of first bytes that were previously interleaved according to first rearranging rules.” The first data columns are rearranged “according to second rearranging rules.”

None of the prior art of record shows or suggests “rearranging an order of bytes of said first data columns according to two or more rearranging rules,” where the first data columns are arranged in plurality of rows. The prior art references mentioned in the instant specification describe interleaving among rows of data in a data block. For example, Fig. 6 shows PO rows added to the bottom of a data block of “data unit” rows. Fig. 7 shows the data block after an interleave operation is performed, where the PO rows are interleaved among the “data units.” By contrast, the present invention includes “rearrangement ... of first data columns” *within* a row, not rearrangement of the rows themselves.

Sollish et al. describe a technique for “for overriding error correction capabilities of digital optical media ... by causing a non-correctable pattern of erroneous symbols to occur in the ECC codeword.” *Abstract*. The inclusion of symbols in the ECC codeword does not suggest modifying any of the prior art cited in the instant specification to perform a step of rearranging an order of bytes of said first data columns.

A further aspect of the present invention is that the rearrangement is performed according to two or more rearranging rules. None of the references of record show or suggest using two or more rearranging rules. None of the references of record show or suggest applying two or more rearranging rules to bytes of said first data columns.

**CONCLUSION**

In view of the foregoing, all claims now pending in this Application are believed to be in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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## **Attachment A**

### **Mark -up copy of amended Specification**

## METHOD OF RECORDING/REPRODUCING DIGITAL DATA AND APPARATUS FOR SAME

### CROSS-REFERENCES TO RELATED APPLICATIONS

- 5 [01] This application is related to and claims priority from Japanese Application No. 2000-371486, filed December 1, 2000 and Japanese Application No. 2000-381652, filed December 11, 2000.

### BACKGROUND OF THE INVENTION

- 10 [02] The present invention relates to an error correction technology to remove an error, in particular, to a digital data reproducing method, a digital data recording method, and apparatus using error correction by product code. In particular, the present invention relates to a data recording and reproducing method, and an apparatus for performing interleave in byte unit to the data consisting of multiple lines.

- 15 [03] Although the present invention is widely applicable to digital data reproducing systems and recording systems that perform error correction by product code, it will be described here by citing a DVD data reproducing system and a data recording system as examples.

- [04] A DVD (digital versatile disc) is a medium which ~~is has~~ about 7 times ~~larger than the~~ capacity of a CD (compact disc) ~~in capacity~~. As a medium that records data on a DVD, there are  
20 DVD-RAM, DVD-R, and DVD-RW. Recordable media are ~~fields most expectable from now~~ ~~on~~ becoming increasingly more popular, as seen in the recent growth of CD-R.

- [05] A format of DVD-RAM will be described below. In a present DVD, interleave is performed per row to the data consisting of multiple lines.

- [06] First, an overview of demodulation processing of ~~data recorded~~ recorded data on DVD-  
25 RAM will be shown by using Fig. 3. The main data 310 that has been recorded is divided per into blocks of 2048 bytes. ~~In each, a~~ As shown in Fig. 4, each block includes 4 bytes of identification data (ID) 401, 2 bytes of IED (ID Error Detection Code) 402 that is an ID error detecting code parity, and 6 bytes of RSV (reservation bytes) 403 that is a reservation area, in

addition to the main data (2048 bytes) for a data stream of 2060 bytes ~~are added~~. Furthermore, 4 bytes of error detecting code parity (EDC) 404 is added to the end of a data stream of 2060 bytes of this data stream, then. The resulting 2064 bytes constitute of data unit 1 (before scramble) 1 (304 and is organized into twelve rows of 172 bytes per row as shown in Fig. 4) ~~is configured~~.

5 Next, according to a scramble rule determined with the value of the ID part of the data unit 1, scramble processing is performed ~~to on the 2048 bytes of the main data part 310 to produce, and~~ it becomes a data unit 1 (after scramble) 1 (305) ~~which is 12 rows x 172 bytes~~. Sixteen instances of these data units (after scramble) 1 are combined to form a data field comprising 192 rows x 172 columns bytes, e.g., (see data field 306 in Fig. 5. Next, 16 rows of Parity of Outer-code (PO) data are added (step 306) to the 192-row data field to produce a 208-row x 172 column data field. Next, ten bytes of Parity of Inner-code (PI) is added (step 307) to each of the 208 rows, extending each row to 182 bytes, to form one ECC block. Then, a PO interleave operation to interleave the sixteen rows of PO data (182 bytes wide) with the original 192-row data field. More specifically, a PO row is added at the end of each instance of data unit 1 (i.e., twelve rows) 15 in the 192-row data field to form sixteen 13-row data units 2 (step 308). After an 8/16 modulation operation is performed to convert the 8-bit data to 16-bit data, twenty-six SYNC codes are added, per one data unit 2 to form sixteen data units 3 (step 309). ~~Furthermore, 16 bytes of Parity of Outer-code (PO) is added to each of 172 columns (lengthwise) of 192 rows x 172 bytes that are configured by 16 data units 1 by making 16 blocks of these data units (after~~ 20 ~~scramble) 1 (305) mutually combined. Next, 10 bytes of Parity of Inner-code (PI) is added to each of 208 rows (widthwise) containing PO to form one ECC block (307) which is a 182 rows x 208 bytes cross Reed-Solomon code. Then, PO interleave which puts each of 16 rows of PO parts (including 16 rows of PI for them) into data units 1 as a 13th row is performed to form 16 data units 2 (308) (that is, one data unit 2 consists of 13 rows). After 8/16 modulation that~~ 25 ~~converts all data into 16 bits from 8 bits is given thereafter, 26 SYNC codes are added per one data unit 2 to form 16 data units 3 (309).~~

[07] Hereafter, each data unit configuration will be described in detail.

[08] First, 2064 bytes of data ~~is are~~ configured ~~by, as shown in Fig. 4, comprising~~ 2048 bytes of main data (310), 4 bytes of identification data (ID401), IED (ID error Detection Code) 402 that is an ID error detecting code parity, 6 bytes of RSV (reservation bytes) 403 that is a reservation area, and 4 bytes of EDC (error Detection Code) 404. A data unit (after scramble) 1

(305) is a data unit ~~by making in which~~ the 2064 bytes of data are organized as twelve rows of ~~into the form of 172 bytes each x 12 rows, where the and scrambling~~ 2048 bytes of main data part are scrambled.

[09] ~~46-Sixteen~~ data units (after scramble) 1 (306) ~~is constitute a 192 rows of 172 bytes each~~  
5 ~~x 192 rows in a data field 306 and are configured by combining 46-sixteen instances of data units~~  
1 (305) as shown in Fig. 5.

[10] An ~~4~~ECC block 307 is a unit of error correction processing in DVD and is a product code (known as a cross Reed Solomon code). The product code ~~will be~~ is formed as follows. As shown in Fig. 6, an outer-code is configured by defining 46-sixteen data units 1 as information  
10 data and making treating each of 172 columns be as RS (208, 192, 17); thus is formed (16 bytes  
rows of parity of outer-code PO\_502 is are added as error correction data). After that, an inner-  
code is formed by making treating the resulting 208 rows including PO\_502 be as RS (182, 172,  
11) in the same direction as the direction of a main data list and the recording direction in a DVD  
(parity of inner-code PI\_501 is added as error correction data). A data unit 2 (308) is a data unit  
15 after the formation of the ECC block 307, and is a 13-row x 182 bytes ~~x 13 rows~~ data unit that is  
configured by inserting interleaving each of the sixteen~~46 rows of PO\_502 into each data unit~~  
including PI\_501 (PO-interleave) among the data units -as shown in Fig. 7.

[11] A data unit 3 (309) is a data train obtained by adding eight kinds (SY0-SY7) of synchronizing signals 801 (SYNC) at the head of each block at every 91 bytes of the data unit 2  
20 as shown in Fig. 8. ~~For example,~~ SY0 (SYNC code 0) in the head of the unit, SY1-SY4  
cyclically inserted in the head of each row, and SY5, SY6 and SY7 inserted for identification of  
each row, and performing 8/16 modulation converting 8-bit data into 16-bit data. Moreover, it is  
possible to identify a position of data, which is reproduced, in the data unit 3 with the generating  
pattern of SYNC 801 from an addition method of this SYNC 801 at the time of reproduction.

[12] After such conversion from the data unit 1 to the data unit 3, data modulated into a  
25 DVD is recorded with NRZI (Non Return to Zero) conversion being performed.

[13] Moreover, the list of main data ~~recorded~~recorded data on the DVD ~~is never~~  
changeddoes not change during the data format conversion process such as scramble, ECC  
encoding, and PO interleave. Hence, the list and sequence of ~~data recorded~~recorded data on the  
30 DVD are equal to the list and sequence of main data.

[14] Therefore, the ~~data recorded~~recorded data on DVD is reproduced in a reverse process of data processing performed in Fig. 3.

[15] Hereafter, conventional data processing at the time of DVD reproduction will be described by using Fig. 9.

5 [16] The 8/16 demodulation is performed while determining a position in the data unit 3 (902) by using SYNC 801, and the data unit 2 (903) is generated. Next, the PO interleave is released-reversed (deinterleaved) while determining a position of the data unit 2 in an ECC block by using ID 401, and an ECC block 901 corresponding to the ECC block 307 before error correction is formed.

10 [17] The reproduction data from the DVD ~~has an error to occur by~~is susceptible to error from various factors. Hence, error correction to a maximum of 5 bytes per inner-code (normally, although each data constituting the code is expressed by “word” or “symbol” in error correction, here, the data is explained by using “byte” as an example of a data unit) is performed in the error correction to inner-code having the same list as a data list recorded in the DVD. The correction  
15 of an error, included in each outer-code, to a maximum of 16 bytes is performed, and error is removed by outer-code error correction. After that, error correction data PI 501 and PO 502 are removed from the ECC block 901, 16 data units 1 (305) shown in Fig. 5 is obtained.

[18] The data of the data unit 1 (305) ~~releases the scrambled~~de-scrambled (304) and is restored into ID, IED, RSV and 2048 bytes of main data (303) again after performing the error  
20 detection processing by using EDC so as to verify that erroneous correction is not performed in the error correction processing.

[19] The above is the overview of the data signal processing at the recording and reproduction of a DVD.

[20] In the error correction processing in the reproduction of a DVD that is described by  
25 using Fig. 9, the error correction of a PI having an identical list with the one of the ~~data recorded~~recorded data in the DVD is performed.

[21] The relationship of data placement on DVD and data placement on ECC block is effective in view of making it possible to correct a comparatively long burst error by performing ~~eraser-error~~error correction, which uses a result as error position information in outer-code error  
30 correction after not letting errors, continuously arising as shown by black parts in Fig. 10C, dispersed, and several uncorrectable error arising in the inner-code error correction. The



vanishing correction method is an error correction method of performing the correction by determining outer-code error positions by using the correction result of the inner-code as described in this specification.

[22] Nevertheless, an uncorrectable error arises in plenty of outer-codes when short burst errors randomly arising as shown by black parts in Fig. 10A pile on in a specific outer-code.  
Error correction is impossible for the burst error in the inner-code error correction, and the number of errors exceeds the number of correctable outer-code. (Figs. 10B and to 10D will be described later.)

[23] Moreover, in connection with the increase of high-density recording data for increasing capacity, one or two bytes of error due to dust and scratches of a current DVD become a short burst error. Thus, ~~a-the average length of time for error concerned-correction~~ (byte length) ~~becomes long~~ increases, and it is estimated that the case that an uncorrectable error arises will increase.

[24] As a countermeasure for these errors, there is an invention disclosed in JP-A-8-125548.

[25] ~~This~~ The invention disclosed in JP-A-8-125548 is a method of making ~~an~~ a burst error dispersed in the entire product code by rearranging the predetermined data in the product code every several bytes. Nevertheless, in the product code having a ratio of inner-code to outer-code like a DVD, there is a problem ~~not to be of~~ not being able to secure correction capability, which is equivalent to a conventional method, for ~~an~~ burst error over ten or more lines. This is because there is a case that, since the burst error is dispersed in the outer-code direction by performing the rearrangement between lines, an area of uncorrectable errors ~~contrarily~~ increases. On the other hand, the present invention does not let an error become dispersed in an outer-code direction because the present invention does not rearrange the data between lines, and hence it is possible to maintain ~~correction capability~~ the ability to correct for the burst error.

[26] Moreover, this is different from the present invention in that a rearrangement range is the entire ECC block and arrangement rules are not changed every line.

[27] Other countermeasures for these errors are described in JP-A-3-266264 and JP-A-9-54956. These inventions are going to raise the tolerance for an burst error by arranging words, included in code words in the column and row directions, so that the words may be mutually apart equally to or more than predetermined distance.

[28] However, this invention is different from the present invention in that this invention does not change arrangement rules every line and performs rearrangement over plural lines, and there is a possibility of not being able to maintain the burst error length.

## SUMMARY OF THE INVENTION

[29] An object of the present invention to provide technology for raising correction capability of a short burst error, which is estimated to increase in future, while securing the correction capability, which is equivalent to conventional technology, for an burst error over several tens of lines.

[30] Major means of the present invention for solving an above subject will be described below.

[31] The present invention is a data recording method of recording data on a record medium, and is intended to improve error correction capacity by rearranging data in sequence per byte for a data train consisting of two or more bytes which constitute the error correcting code for recording data on this record medium and recording the data on the above-described record medium.

[32] In addition, the present invention is intended to improve the error correction capacity by rearranging data per byte in sequence for parts of a data train except identification information out of the data train consisting of two or more bytes which constitute the error correcting code for recording data on this record medium, and recording the data on the above-described record medium.

[33] Moreover, the present invention is intended to improve the error correction capacity by generating error correcting code through adding error correction data to the data for recording on this record medium, rearranging data, forming this data train, per byte about the data train which constitutes this error correcting code, demodulating the data train which is rearranged in its sequence for data per byte, and recording the modulated data train on the above-described record medium.

[34] Further, the present invention is a data reproducing method that reproduces the data modulated and recorded on the record medium. The present invention is intended to improve the error correction capacity by demodulating the data train recorded on the record medium, restoring the data train, which is demodulated and rearranged according to the predetermined

rule, to the data train in the sequence before being rearranged per byte for data forming the data train, correcting the errors that are included in the error correcting code restored to the data train in the sequence before being rearranged, and reproducing the data whose errors are corrected.

[35] Furthermore, the present invention is a data recording apparatus recording data on a record medium. The present invention is intended to improve the error correction capacity by the data recording apparatus which comprises a circuit generating error correcting code for recording data on the record medium, a signal processing circuit which rearranges sequence for data per byte about a data train which consists of two or more bytes which constitutes the error correcting code, and a modulation circuit which modulates the data train which are rearranged in its sequence for data per byte.

[36] Still further, the present invention is a data reproducing apparatus that reproduces data modulated and recorded on a record medium. The present invention is intended to improve error correction capacity by a data reproducing apparatus characterized in comprising a demodulation circuit which demodulates the data train recorded on the record medium, a signal processing circuit which restores the data which forms a the data train to the data train in the sequence before being rearranged in the sequence per byte about the data train that is demodulated by the demodulation circuit and is rearranged according to a predetermined rule, an error correcting circuit which corrects the errors included in the error correcting code restored to the data train before being rearranged by the signal processing circuit, a reproducing circuit which reproduces the data which had the error corrected by the error correcting circuit.

[37] Thus, when the byte interleave for each row (here, the row ~~talks noting that it has the~~ same list as the data list recorded on the record medium) of a product code is performed under a rule different every row, that is, when data rearrangement is performed according to the rule which is different every inner-code of the ECC block 307 in a DVD, several bytes to several tens bytes of short burst error is dispersed in degree different every row. Hence, conventional errors shown in Fig. 10A become errors shown in Fig. 10B. Since an error count is equalized on outer-code in Fig. 10B even if uncorrectable errors are generated in the outer-code error correction in Fig. 10A, the probability of further decreasing the errors included in data by the outer-code error correction becomes high.

[38] This effect means that it becomes possible to obtain characteristics of error correction still better than those of a current DVD by performing the repetitive decoding, which performs

the same error correction repeatedly again, after performing error correction to inner-code and error correction to outer-code that are effective to random errors.

[39] Furthermore, if performing interleave processing within each row of the product code, it becomes possible to secure the burst correction length the same as the former. This is because data dispersion does not occur in the direction of line of data formed by outer-code, even if the error generated like Fig. 10C is set to Fig. 10D by the byte interleave.

[40] Thus, in the present invention, an error count is equalized even at the time of an uncorrectable error arising conventionally, without changing burst correction length by performing the byte interleave every row of a product code under a rule different every row, rearranging the data by using a rule different every row, and making the data dispersed so that several bytes to several tens bytes of short burst error may have not correlation. Hence, the probability that more errors can be corrected becomes high. Moreover, in many cases, in the repeat correction having the excellent capacity to a random error, it also becomes possible to correct errors more than those in the past in a repeat count equal to or less than that in the past.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[41] Fig. 1 is a block diagram showing a data processing flow at the time of recording when the present invention is applied to a DVD;

[42] Fig. 2 is a diagram showing an example of PI interleave;

[43] Fig. 3 is a block diagram showing a data processing flow at the time of recording of the DVD;

[44] Fig. 4 is a diagram showing a data unit 1 after scramble;

[45] Fig. 5 is a diagram showing 16 data units 1 after scramble;

[46] Fig. 6 is a diagram showing an ECC block;

[47] Fig. 7 is a diagram showing 16 data unit 2;

[48] Fig. 8 is a diagram showing a data unit 3;

[49] Fig. 9 is a block diagram showing an example of a data processing flow at the time of reproduction of the DVD;

[50] Figs. 10A-10D are drawings showing an effect at the time of PI interleave for a short burst error and a long burst error;

[51] Fig. 11 is a diagram showing one ECC block after PI interleave;

- [52] Fig. 12 is a block diagram showing a data processing flow at the time of reproduction when the present invention is applied to the DVD;
- [53] Fig. 13 is a diagram showing an example of processing for canceling PI interleave (deinterleave);
- 5 [54] Fig. 14 is a diagram showing an example of a data unit 2 after PI interleave;
- [55] Fig. 15 is a block diagram showing an example of a DVD recording and reproducing apparatus to which the present invention is applied;
- [56] Figs. 16A and 16B are block diagrams showing examples of M-series generating circuits;
- 10 [57] Figs. 17A and 17B are block diagrams showing examples of M-series generating circuits;
- [58] Figs. 18A and 18B are block diagrams showing examples of constituting each address generating circuit by using an address decoder;
- [59] Fig. 19 is a block diagram showing an example of a PI interleave circuit;
- 15 [60] Fig. 20 is a block diagram showing an example of a PI deinterleave circuit (circuit which cancels PI interleave);
- [61] Fig. 21 is a block diagram showing an example of PI interleave being performed for two inner-codes under one PI interleave conversion rule;
- [62] Fig. 22 is a block diagram showing an example of PI interleave being performed every  
20 two bytes to one inner-code;
- [63] Figs. 23A and 23B are block diagrams showing examples of respective M-series generating circuits;
- [64] Fig. 24 is a block diagram showing an example of an arithmetic progression generating circuit;
- 25 [65] Fig. 25 is a block diagram showing an example of a PI interleave circuit; and
- [66] Fig. 26 is a block diagram showing an example of a PI de-interleave circuit (circuit which cancels PI interleave).

## DESCRIPTION OF THE EMBODIMENTS

[67] Hereafter, the present invention will be described by using drawings. Here, the present invention will be described by making a DVD data reproducing system, and a data recording system be examples.

5 [68] Fig. 1 shows an example of showing data processing steps at the time of recording when the present invention is applied to a current DVD logical format shown in Fig. 3.

[69] Fig. 1 will be briefly described. The main ~~data recorded~~ recorded data 310 is divided ~~per~~ into 2048 bytes. In each head, as shown in Fig. 4, 4 bytes of identification data (ID) 401, IED (ID error Detection Code) 402 that is ID error detecting code parity, and 6 bytes of

10 RSV (reservation bytes) 403 that is a reservation area are added. Furthermore, 4 bytes of error detection code parity (EDC) is added to 2060 bytes of this data stream, then 2064 bytes of data unit (before scramble) 1 (304) is ~~configured~~ organized into twelve rows of 172 bytes each. Next, according to a scramble rule determined with the value of the ID part of the data unit 1, scramble processing is performed ~~to on the~~ on the 2048 bytes of the main data part, ~~and it becomes to produce a~~

15 data unit (after scramble) 1 (305) which is ~~12~~ twelve rows x 172 bytes. Furthermore, ~~16~~ sixteen rows of Parity of Outer-code (PO) data is added to a 192 row x 172 byte data field comprising each of 172 columns (lengthwise) of 192 rows x 172 bytes that are configured by 16 sixteen data units 1 (306), to produce a 208-row data field by making 16 blocks of these data

units (after scramble) 1 (305) mutually combined. Next, ~~10~~ ten bytes of Parity of Inner-code (PI) is added to each of ~~the 208 rows (widthwise) containing PO~~ the 208 rows to form one ECC block (307) which is a ~~182 rows x 208 bytes~~ 208 row x 182 byte cross Reed-Solomon code. Next, in a PI interleave operation, the data in each row of the ECC block is rearranged ~~every one on a byte-by-byte basis~~

according to each rule to obtain an interleaved ECC block 101. Then, a PO interleave operation interleaves which puts each of the 16 rows of PO parts (including 16 rows of and PI for them)

25 data among the ~~into sixteen~~ into sixteen data units 1 as a ~~13th row is performed to form 16 data units 2 (102) (that is, one data unit 2 consists of 13 rows) of the original 192 rows in the data field~~. Then, after 8/16 modulation ~~that is performed to converts all data into 16 bits from 8 bits is given, followed by the incorporation of twenty-six~~ 26 SYNC codes are added per one for each data unit 2 to form 16 data units 3 (103).

[70] However, although PI interleave is performed immediately after ECC block generation in Fig. 1, naturally, it is no problem to perform PI interleave after constituting the data unit 2, or after constituting the data unit 3.

[71] Moreover, the “word” and the “symbol” which are the unit of data are also described as a “byte” here.

[72] In Fig. 1, the added PI interleave operation is a means-byte interleave processing operation based on a certain rule for rearranging the sequence on the basis of a certain rule for of 182 bytes of data (inner-code) of each row in the ECC block of DVD as shown in Fig. 2. That is, the added PI interleave operation shows the processing for rearranging the byte sequence about the data train which consists of a plurality of bytes constituting error correcting code. Here, the data train means an inner-code forming the ECC block, that is, an arrangement of the data in the row direction. At this time, the effect in the point of dispersion of errors becomes large by using conversion rules (interleave rules,  $F_i(x)$ )  $F_i(x) (=y)$  that have no correlation and are different from one another in the 208 rows of inner-code included in the ECC block. However, it is possible to obtain the effect of error dispersion even if this PI interleave is performed by using at least two kinds of conversion rules (interleave rules)  $F_1(x)$  and  $F_2(x)$ . Moreover, data  $D_{i, 0}; D_{i, 1}; D_{i, 2}; \dots; D_{i, 181}$  show the data constituting the inner-code in the  $i$ -th row of an ECC block, and  $D_{i, 171}; D_{i, 172}; \dots; D_{i, 181}$  correspond to the parity of inner-code PI.

Therefore, the data train (B) generated by performing PI interleave operation ~~to on~~ the data train (A) is not always inner-code.

[73] It is also possible to perform PI interleave, which rearranges the record sequence of this data, among a plurality of inner-codes. In this case, although it becomes possible to obtain still higher correction capacity to a random error, burst error length become short.

[74] Fig. 11 is a diagram showing an ECC block (101) after performing the PI interleave shown in Fig. 1. This shows the status that each row of the ECC block shown in Fig. 6 is given PI interleave and is transformed.

[75] Fig. 12 shows a data conversion flow at the time of recording data, generated after performing the data conversion process shown in Fig. 1, on a DVD and reproducing the data.

[76] In Fig. 12, a data unit 2 (1203) is generated from the data that is recorded on the DVD while determining the position in the data unit 3 by using SYNC801, and performing 8/16 demodulation. Next, a PO deinterleave operation is performed to produce an ECC block (1201)

which is given PO interleave processing and is shown in Fig. 11, is formed by canceling PO interleave while determining the position of the data unit 2 in the ECC block 307 by using ID401. The PO deinterleave operation is the inverse of the operation shown in Fig. 1 where the PO row was inserted after every twelfth row. Then, the ECC block (1201) is restored to an ECC block (901) shown in Fig. 6 by applying the conversion rule  $G_i(y) \rightarrow G_i^{-1}(y)$ , which is the inverse transformation of  $F_i(x) \rightarrow F_i(x)$  and is shown in Fig. 13. Thus, the bytes in each row are reorganized according to the inverse function  $G_i(y)$  to restore, that is, performing every row PI deinterleave which performs conversion of restoring again the symbol train (A), obtained by data rearrangement at the time of modulation, to PI code from the symbol train (B). After this, as usual, an error of up to 5 bytes is corrected in each inner-code by the error correction to inner-code, and an error of up to 16 bytes, included in each outer-code, by the error correction to outer-code is corrected (306). Then, ID, IED, RSV, and 2048 bytes of main data (303) are obtained again after removing the data PI and PO for error correction required for error correction processing, restoring the ECC block to the 16 data unit 1 (305) shown in Fig. 5, canceling scramble (304), and performing error detection processing by using EDC. In addition, as for conversion rules  $F_i(x) \rightarrow F_i(x)$  and  $G_i(y) \rightarrow G_i^{-1}(x)$ , the apparatus may have the information as rules defined beforehand. Alternatively, the conversion rules  $F_i(x) \rightarrow F_i(x)$  and  $G_i(y) \rightarrow G_i^{-1}(x)$  may be recorded every on the medium itself, and the apparatus may read the information. In the latter case of the latter, it is possible to perform the above-described processing after reading conversion rules  $F_i(x) \rightarrow F_i(x)$  and  $G_i(y) \rightarrow G_i^{-1}(x)$  first, and to determine the conversion rules  $F_i(x) \rightarrow F_i(x)$  and  $G_i(y) \rightarrow G_i^{-1}(x)$  for every disk unit, ECC block unit, frame unit, or the like in the apparatus.

[77] However, in the demodulation process shown in Fig. 12, the position in the ECC block is determined by using the ID. Thus, if a PI interleave operation is performed where the interleave function  $F_i(x)$  varies for each row, it is not possible to determine  $x=G_i(y)$  at the time of restoring a data train since a conversion rule  $y=F_i(x)$  for PI interleave for a row including ID cannot be found. Hence, it becomes very difficult to seek the ID. However, as shown in Fig. 12, in case demodulation processing is usually performed in DVD used as an example in this explanation, the position in the ECC block is determined by using ID. Hence, when PI interleave which is different in every row of all ECCs is applied, if PI interleave processing at the time of record is applied, it is not possible to determine  $x=G_i(y)$  used in PI deinterleave at the time of



~~restoring a data train since a conversion rule  $y = F_i(x)$  for PI interleave for a row including ID cannot be found. Hence, it becomes very difficult to seek the ID.~~

[78] Therefore, the information showing the position in a product code is shown, that is, ID and IED (IED is also required when the reliability of ID is required) are removed from the objects of not subjected to any data interleave operation on a DVD. Consequently, and rows including this information are given subject PI interleave processing by processing only to 176 bytes (e.g., bytes 7 through 182) of data except and leave the 6 bytes of identification information such as ID and IED unaltered.

[79] When this is applied to a DVD, the data unit 2 (102) shown in Fig. 1 becomes as shown in Fig. 14. In this case, identification information containing EDC, RSV, etc. cannot be obtained until the code is decoded into the original inner-code by performing PI deinterleave since all the data except ID and IED are set as the objects of scramble.

[80] Therefore, although the effect of PI interleave becomes a little weak when the information which is needed before forming an ECC block in RSV etc. at the time of reproduction is included, it is necessary to remove the data as well as ID from the objects of the interleave.

[81] Moreover, as shown in Fig. 14, if removing ID and IED from the objects of PI interleave, in regard to the conversion rules  $F_i(x)F_i(x)$  of the inner-code including ID and IED, it is assumed that  $x = 1, \dots, 182$  and the values of  $x$  show position addresses as shown in Fig. 2.

Then it should function can be devised revised to become so that  $F_iF_i(n) = n$  (for  $n = 1, 2, 3, 4, 5$ , and 6), or it is the function can be made to limit  $x$  and  $F_i(x)$  to be in a range of 6 to 182.

[82] Fig. 2 on which is briefly touched above will be described again. Fig. 2 is an example of a diagram having shown the method of a data list at the time of adopting PI interleave with the conversion rule  $F_i(x)F_i(x)$  for PI interleave to the inner-code described in Fig. 6 where the present invention is described above. An inner-code is 182 bytes of data train, data (A) denotes the inner-code after the addition of PI and PO, and data (B) denotes 182 bytes of data train which is given PI interleave by the conversion rule  $F_i(x)F_i(x)$  and is rearranged in the sequence of data thereof. Here, although the data (B) is an example of rearranging data every 13 pieces, the conversion rule  $F_i(x)F_i(x)$  is not limited to this, but is enough to discontinuously rearrange the data.

[83] Two or more kinds of conversion rules  $F_i(x)F_i(x)$  are prepared in order to perform different values of PI interleave. In a DVD, the conversion rules of up to 208 kinds are prepared, and error counts on outer-codes in an ECC block are equalized as shown in Figs. 10A to 10D by applying the different conversion rule for every inner-code. Hence, cases that error correction to  
5 outer-codes become possible increases. Thus, it becomes possible to increase correction capacity by performing different PI interleave to the inner-codes and recording the inner-codes on a record medium. Moreover, this effect becomes still larger when the code is decoded repeatedly.

[84] Next, a method of implementing the conversion rule for this PI interleave in a circuit will be described. First, an example of a configuration of a DVD recording and reproducing  
10 apparatus at the time of applying according to the present invention will be described by using Fig. 15. Although a recording and reproducing apparatus is described as an example here, thea present invention is applicable also to a reproduction dedicated device and a record dedicated device.

[85] An optical pickup 1502 performs record and reproduction of data on a record medium  
15 1501 such as a DVD, and a spindle motor 1503 rotates a disk. Moreover, a servo 1504 controls the optical pickup 1502 or the like. A read channel 1505 performs waveform equalization and doubling of an analog reproductive signal read from the record medium 1501, and synchronous clock generation. A decoder 1506 consists of a demodulation circuit 1507 performing 8/16 demodulation of data read, and an error correcting circuit (1508, 1518) performing the  
20 processing of removing errors included in the data, and RAM 1509a temporarily stores the data at the time of reproduction. RAM 1509b temporarily stores the data at the time of record. This can be also used as the RAM 1509a. Numeral 1514 is a laser driver. A modulation circuit 1512 performs the modulation of the data at the time of record, and an encoding circuit 1513 consists of an error correcting code generation circuit adding parity of error correcting code, PI and PO,  
25 and a scramble circuit performing scramble processing. An interface 1515 controls the input/output of data with a host system, and a microcomputer 1516 generalizes the system. In addition, it is also possible to use a microcomputer as the error correcting code generation circuit adding the error correcting code parity PI and PO.

[86] A PI interleave circuit (signal processing circuit which rearranges the data in an inner-  
30 code as shown in Fig. 2) 1517 implements the present invention, and a PI deinterleave circuit 1518 is a signal processing circuit which performs cancellation of PI interleave and processing

shown in Fig. 13. That is, the PI interleave circuit 1517 rearranges the sequence of word bytes for the data train which consists of a plurality of word bytes who constitutes an error correcting code, and the PI deinterleave circuit 1518 restores the data train, which is rearranged, to the data train in the sequence before being rearranged.

5 [87] The PI interleave circuit 1517 has SRAM and a register which can store at least 182-byte data in a system where PI interleave closed within one inner-code is performed. Hence, the PI interleave circuit 1517 reads data every inner-code from the RAM 1509b after ECC block generation at the time of record, and temporarily stores the data in the sequence at the time of being read, that is, in the form of an inner-code in the register. After that, the PI interleave  
10 circuit 1517 writes the data on the register again in RAM 1509b while converting the data list according to predetermined PI interleave conversion rules.

[88] The PI deinterleave circuit 1518 has SRAM and a register which can store at least 182-byte data in a system where PI interleave closed within one inner-code is performed. At the time of the reproduction after data is read from a DVD, the PI deinterleave circuit 1518 reads data  
15 from the RAM 1509a every inner-code immediately after 8/16 demodulation and temporarily stores the data in the register in the present sequence. After that, the PI deinterleave circuit 1518 writes the data on the register again in RAM 1509a while converting the data list according to predetermined PI interleave conversion rules. Moreover, similar processing can be also performed in the following configuration. That is, in the PI deinterleave circuit 1518, the  
20 numbers of SRAM and registers are increased, and arranged just after the demodulation circuit in the decoding circuit 1508, and the data outputted from the demodulating circuit is directly inputted into the register so that the data train having the byte count equivalent to the count of the inner-code is arranged. Then, the PI deinterleave circuit 1518 arranges the data, saved in the register, in the RAM 1509a while performing PI deinterleave of the data.

25 [89] Next, a PI interleave circuit and a PI deinterleave circuit that are shown in Fig. 15 will be described. Fig. 19 shows an example of the PI interleave circuit 1517 where PI interleave conversion rules are defined by using the M-series generating circuit 1901-~~f~~, which is a circuit generating that generates the maximum periodic column, ~~and, e.g.,~~ the maximum period column (~~[=]~~referred to as the M-series) is 255 ~~at the time in the case~~ of using an 8-bit register (i.e.,  $2^8-1$ ).  
30 Moreover, here, it is assumed that the inner-code read from the RAM 1509b has been already stored in a shift register 1902. As write control signals to the RAM 1509b, there are a write

request signal, an address (however, referred to as 1 to 182 for convenience here) in the RAM 1509b, and write data. When the write request signal is outputted, a write request acknowledge signal, which shows that data is written, is inputted from the RAM 1509b.

[90] In this circuit, when the write request acknowledge signal is inputted, that is, the timing when the data is written, the shift register 1902 shifts. Moreover, the M-series generating circuit 1901 also changes to the following value if the write request acknowledge signal is inputted, or if the signal of 1 to 255 generated by the M-series generating circuit 1901 exceeds the address to be required, i.e., if the signal has the value of 183 or more. Here, the value range is not necessary to be 1 to 255. In a DVD, the inner-code is 182 bytes, and PI interleave in the data in all the inner-codes is concerned here. Hence, an output from the 8-bit M-series generating circuit is used. Moreover, the write request signal is outputted when the address made in the M-series generating circuit 1901 is ~~judged~~determined to be 182 or less by a request generation judging circuit 1903.

[91] This is to make an address skipped if the address made in the M-series generating circuit 1901 exceeds 183, because PI interleave processing cannot be performed.

[92] Fig. 20 shows an example of the PI deinterleave circuit 1518 where PI interleave conversion rules are defined by using the M-series generating circuit 1901. Moreover, here, it is assumed that the data train read from the RAM 1509a has been already stored in a register 2001.

[93] As write control signals to the RAM 1509a, there are a write request signal, an address in the RAM 1509a, and write data. When the write request signal is outputted, a write request acknowledge signal, which shows that data is written, is inputted from the RAM 1509a.

[94] In this circuit, when the value of the same M-series generating circuit 1901 as the M-series generating circuit 1901 where the PI interleave conversion rules are defined exceeds 183, the following value is outputted from the M-series generating circuit 1901. When the value is 182 or less, a write request is generated, and one byte of data in the data train chosen with the value of this M-series generating circuit 1901 is written in the address which a counter 2002 shows. Moreover, since a write request acknowledge signal is inputted when writing is performed, the counter 2002 which generates an address shows the following value, and the M-series generating circuit 1901 also shows the following value.

[95] In this circuit also, it is necessary to ~~make-skip~~skip an address ~~skipped~~ if the address made in the M-series generating circuit 1901 exceeds 183, because PI deinterleave processing cannot be performed.

[96] Moreover, in these circuits, if an address is 1 to 6 in the request generation judging circuit in the inner-code containing ID, the address is treated similarly to a case of being 183 or more. When overwriting the data train, which is given PI interleave, to the original inner-code of the RAM 1509b, i.e., the inner-code stored in the register 1902, it is not necessary to write ID and IED in the RAM 1509b. Moreover, when storing the data train in another area of the RAM 1509b, a system writing ID and IED in a predetermined position is added.

[97] However, a countermeasure for the inner-code containing ID can be easily achieved by adding an offset to an address, or the like.

[98] Many kinds (208 or more kinds required of PI interleave conversion rules which are different in all inner-codes in a DVD) of M-series defining PI interleave rules that are used in Figs. 19 and 20 can be generated in the following combination.

[99] This can be easily implemented by combining the following items 1 and 2.

[100] 1. Changing of the kind of feedback of the shift register generating M-series (corresponding to the relation between Figs. 16A and 16B).

[101] 2. Rearrangement of the position of data outputted from the shift register (corresponding to the relation between Figs. 16A and 17A).

[102] For example, it is assumed that the positions of the data outputted from the shift register in 13 inner-codes in the data unit 2 are rearranged by changing the feedback rules of the M-series generating circuit every unit of the data unit 2 in Fig. 1, i.e., every unit of the data unit in Fig. 14.

Then, it is possible to obtain 208 kinds of different PI interleave conversion rules.

[103] Moreover, different M-series can be also generated by changing the polarity value of a certain bit as shown in Fig. 17B. However, since zero may be outputted from M-series in this case, and a value at the time of the register being zero and an address is not generated at the value "AA=170" in hexadecimal notation in Fig. 17B, it becomes necessary to ~~perform such a~~ devise that an address is calculated by subtracting 0x170 from the obtained value to produce a suitable address. However, these can be used as M-series that define PI interleave rules.

Moreover, similarly, it is clear that an address can be converted by using a logic circuit obtained by combining OR, AND, and NOT.

[104] As shown in Fig. 23A, values obtained by adding values different in every row (however the same row fixed value) to the value outputted from each M-series generating circuit 1901 in Figs. 16A, 16B, 17A, and 17B that are shown above are also M-series. Hence, the M-

series can be used as PI interleave conversion rules according to the present invention. However, in this case, a carry to the ninth bit (MSB) that is generated by performing addition is ignored.

[105] Moreover, values obtained by substituting a multiplier 2303, as shown in Fig. 23B, for an adder 2302 in this diagram, and multiplying the fixed value corresponding to each row on a finite field GF (28) are also M-series. Hence, the M-series can be used as PI interleave conversion rules according to the present invention. A line-counter 2301 counts the position of the inner-code in a product code, i.e., a line address.

[106] As a method of generating a plurality of PI interleave conversion rules that is for achieving the object of the present invention to performs PI interleave, that is, for making burst errors, produced at random per several bytes, equally dispersed in all outer-codes, and is a simplest circuit, there is a method of changing the initial value of the M-series generating circuit 1901 shown in Fig. 19 according to a row. This means that M-series generated by the same M-series generating circuits 1901 are generated by shifting the M-series. As an example, there is a method of substituting a row address as the initial value of each PI interleave conversion rule.

Thereby, at least 182 kinds of PI interleave conversion rules are generated. However, in order to use PI interleave conversion rules which are different in all 208 rows, it is necessary to combine this method with another PI interleave conversion rule generating method. In addition, as long as a method can change M-series according to a row, the method besides the above-described examples can be used.

[107] It is also possible to realize the PI interleave circuit 1517 and PI deinterleave circuit 1518, which are shown in Fig. 15, with another method without using the M-series generating circuit 1901.

[108] This is a method of realizing PI interleave conversion rules with ROM or a circuit as shown in Figs. 18A and 18B instead of the M-series generating circuit 1901. In particular, this is effective when only several kinds of PI interleave conversion rules are necessary. Moreover, a still higher effect is expectable in that an address can be set freely such that PI interleave rules are managed with the distance between data adjacent to each other in an inner-code in order to advance random characteristics.

[109] Moreover, there is a method of using arithmetic progression as a method except methods using M-series as PI interleave conversion rules.

[110] Here, since what is necessary is just to use 182 arbitrary numbers as PI interleave rules in a DVD as PI interleave rules, suppose that numbers 0 to 181 are used.

[111] This is a method of rearranging the list of an inner-code according to arithmetic progression, for example, rearranging positions of the data in the inner-code according to PI interleave rules, that is, 0, 3, 6, 9,..., 177, 180, 1, 4, 7, ..., 178, 181, 2, 5, 8, ..., 176, 179 in the case of using a progression where numbers increases by 3.

[112] In this case, it is necessary to use a constant, which is different in each row, as an increment. Nevertheless, when numbers that are coprime to 182 are used as constants, in regard to numbers exceeding 181, values obtained by subtracting 182 from the numbers can be used as the constants. However, when numbers that are not coprime to 182 are used as constants, for example, when the increment is 2, the numbers become 0, 2, 4, 8, ..., 180, 0, 2, 4, ..., and hence it becomes necessary to provide a system of adding one when exceeding 182 so that the same numbers may not appear twice.

[113] Moreover, if most target burst errors generated at random are 10 bytes or less, it is better to choose 11 or more as an incremental constant.

[114] However, when 182 bytes are selected as an inner-code when an arithmetic progression is used, it is necessary to note that the case where one is selected as a constant and the case that 181 is selected as a constant are the same in an object of dispersing errors in the different outer-codes.

[115] This is because adjacent numbers become the same although there is difference between the left and the right since the list becomes 0, 1, 2, 3, 4, ..., 181 when one is selected as a constant, and the list becomes 0, 181, 180, ..., 4, 3, 2, 1 when 181 is selected.

[116] An example (only numbers that are coprime to 182 except one are used) of the circuit that generates an arithmetic progression is shown in Fig. 24.

[117] In this diagram, an incremental constant is selected and used by being switched according to the value of a row address changed and is used so that values outputted from an 8-bit register 2401 becomes an arithmetic progression and a different series as much as possible may be obtained according to an inner-code, that is, according to a row.

[118] Moreover, Figs. 25 and 26 show examples where arithmetic progressions are applied to the PI interleave circuit 1517 and PI deinterleave circuit 1518 in Fig. 15. This can be configured

only by replacing the M-series generating circuit 1901 in Figs. 19 and 20, which is described above, with the arithmetic progression generating circuit 2501 in Fig. 24.

[119] The circuit in Fig. 19 is cited as an example of the M-series generating circuit 1901 of the PI interleave circuit 1517 in Fig. 15, and the method of arranging data in the addresses which corresponds to an M-series every one byte from a head of the data in an inner-code is shown. However, there is a method of arranging the data, stored at the positions on the inner-code generated by the M-series, in order of the M-series by using the PI deinterleave circuit 1518 in Fig. 20 as the PI interleave circuit 1517.

[120] Moreover, Fig. 19 shows the PI deinterleave circuit 1518 corresponding to this.

[121] Naturally, when a different M-series is used and this method is also used, the object to disperse burst errors on different outer-codes can be attained.

[122] However, when this method is used, burst errors cannot be dispersed on different outer-codes by changing the initial value of an M-series in each row.

[123] The relation between two kinds of these PI interleave methods are the same as the arithmetic progression generating circuits 2501 described by using Fig. 25 showing the PI interleave circuit 1517 and Fig. 26 showing the PI deinterleave circuit 1518.

[124] PI interleave conversion rules can be configured by some combinations containing the M-series and arithmetic progression, which are introduced above, as well as one method, and the circuit which realizes them can be also realized by the combination of respective elements.

[125] Moreover, it is also good to combine address decoders 1801 and 1802 constituted by the M-series generating circuit 1901, ROM, and circuits in order to generate many PI interleave conversion rules.

[126] Moreover, in order to take PI interleave conversion rules into consideration from a circuit and to perform transform processing at high speed, as shown in Fig. 21, it is possible to simultaneously perform a plurality of PI interleave by using the same conversion rule. It is also possible to simultaneously perform two or more bytes (2 bytes in Fig. 22) of PI interleave within the same inner-code, as shown in Fig. 22. That is, it is possible to make two or more bytes be a group, and to rearrange the order of groups by a group.

[127] When these are actually implemented into circuits, the optimal PI interleave method can be selected in consideration of the bus width of RAM, and data allocation according to processing speed required. In addition, it is necessary to also take into consideration of the



circuit scale at the time of implementation, and the degree of performance improvement obtained by the present invention.

[128] Moreover, although these diagrams show examples at the time of performing PI interleave by 2 bytes unit, three or more are sufficient as the size of the inner-code to which the same PI interleave is actually applied.

[129] Although cases where the present invention is applied to a DVD are described through embodiments, the present invention is effective at a digital data recording and reproducing apparatus, including a product code, and a digital data recording and reproducing method.

[130] In addition, it should be noted that, when recording to a record media is performed according to the list of the outer-code in a product code, the inner-code used in the explanation corresponds to the outer-code. Moreover, although the signal processing circuit using an M-series and an arithmetic progression is exemplified in the PI interleave circuit 1517 and PI deinterleave circuit 1518, other pseudo-random number generating circuits or the like can be used.

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